PATENT SPECIFICATION (11) 1 512 220

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(21) Application No. 44698/75 (22) Filed 29 Oct. 1975
(31) Convention Application No. 213 526
(32) Filed 12 Nov. 1974 in
(33) Canada (CA)
(44) Complete Specification published 24 May 1978
(51) INT CL² G06F 11/00
(52) Index at acceptance G4A 11B 12T 13E 6H ES

(19)

(54) A METHOD OF PROVIDING A SUBSTITUTE MEMORY MODULE

(71) We, NORTHERN TELECOM LIMITED formerly known as Northern Electric Company Limited, a Canadian Company of 1600 Dorchester Boulevard, West Montreal, Quebec, Canada, H3H 1R1, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

Field of the Invention

The present invention relates to data processing systems in general and in particular to the utilization of memory modules therein.

Background of the invention

In recent years the trend in telephone apparatus and systems has been towards increased computerization. As a result many such systems of modern design contain data processing sub-systems to perform supervision and control functions in lieu of the hitherto extensively used electromechanical devices.

The requirements placed on telephone systems are in certain aspects sometimes in conflict with the performance specifications of conventional data processing systems. Certainly the most prominent example of such conflict arises due to the extreme reliability requirements placed on telephone systems and apparatus. In contrast, occasional failure of a computer, be it because of hard or software malfunction, is not uncommon.

While often higher reliability on telephone systems is attained by duplicating critical units of the system, such approach is in conflict with yet another important requirement, that of cost.

The present invention discloses a method of inexpensively providing spare memory capability in a data processing system at the cost of slightly reducing its normal functional capability. The present invention is particularly suitable for use in certain types of telephone systems. It is, however, not restricted to such use, as will be apparent to those skilled in related arts.

Summary of the Invention

The method of the present invention is applicable in a data processing system having a plurality of separately callable memory modules each having an address. The method permits substitution of one memory module for another and comprises the steps of: electronically marking one memory module as a spare or substitute module; entering into an address register the address of another memory module upon fault detection in that other memory module inhibiting the substitute memory module from responding to its address; continuously comparing called addresses of memory modules with the address stored in the address register; and, upon occurrence of a match between a called address and the address in the register, selecting the substitute memory module instead of the called memory module.

Usually the memory module marked as a substitute module would be one of low priority and/or low utilization probability (for example due to it having a high address in a read/write or scratch-pad memory) compared with the remaining modules. The substitute memory module is loaded with data substantially identical to that of the faulty module after the fault has been detected. In a preferred embodiment, this is accomplished by reading the appropriate portion of an auxiliary standby storage tape containing the data vital to the system. This, of course, occurs under the control of the CPU (Central Processing Unit) in the system in a well known manner, Clearly, all other control functions such as fault location among memory modules, the calling of memory module addresses and the loading of the address of the faulty memory module into the address register are initiated by the CPU.

Any interruption of service due to the

process of loading the substitute module will depend on the type and capacity of the module and should be of the order of minutes which is still better than total failure.

Brief Description of the Drawings

An example embodiment will now be described in conjunction with the drawings in which:

Figure 1 is a block schematic diagram of a multi-line, multi-station telephone exchange system capable of increased reliability according to the present invention; and

Figure 2 is a block schematic diagram of a circuit embodying the method of the present invention is utilized in the system of Figure 1.

Description of the Preferred Embodiment

The method of the present invention is utilized in a multi-line, multi-station telephone exchange system which performs internal switching functions as well as connects local station sets with an exchange office of the telephone network. The outline of a typical system is shown schematically in Figure 1 of the drawings. It comprises a plurality of station sets S1 and Sn which are centrally connected to a peripheral equipment unit P1. The unit P1 is in turn connected to a control unit CU which contains a central processing unit CPU that (among other tasks) controls access to a standby magnetic tape storage unit MT and a system memory SM. For clarity of description, Figure 1 shows only essential elements of the system that are necessary for understanding the present invention.

The system memory SM is shown in Figure 2 of the drawings in more detail. Again for reasons of clarity and ease of understanding, the system memory is shown with only three constituent memory modules M1, M2 and M3. Each memory module is callable via an address bus 100 by a unique individual address, the individual addresses being decoded in address decoder logic units 10, 11 and 12 which in turn enable the associated data store upon the occurrence of a match between the stored memory module address and the called address. The data into or from data stores 21, 22 and 23 is usually written or read from or onto a common data bus. The address decoder logic unit 10 is shown in block schematic and comprises a module address store 101 supplying the module address to a comparator 102 which compares the same with the called address on address bus 100. The result of the comparison is fed to an AND-gate 103, which is also driven by an OR-gate 104. One input of the OR-gate 104 is driven from a spare-in-use bus 300 via an inverter 105. The other input of the OR-gate 104 is driven from an AND-gate 106, one input of which is driven from spare marker 107 via an inverter 108. The other input of the AND-gate 106 is driven from a select-spare bus 200 via an inverter 109. The spare marker 107 also drives an AND-gate 110, also driven by the select-spare bus 200. The output of the AND-gate 110 as well as that of the AND-gate 103 drives an OR-gate 111 which enables (and disables) the data store 21.

An address register 400 is controlled from the CPU of the system and is adapted to receive the address of a faulty memory module. One bit in the address register 400 is set to logical "1" when the register is being loaded with an address; it is termed spare-in-use bit and drives the spare-in-use bus 300. The contents of the address register 400 are input to a comparator 500 which continuously compares the address in the register 400 (if any) with the called address on the address bus 100. The result is output on the select-spare bus 200. The address bus 100, the spare-in-use bus 300 and the select-spare bus 200 all are inputs to each of the memory modules M1, M2 and M3.

Now the method of operation of the system will be described step by step. Assuming the memory module M1 is a low priority module and has been selected to be the substitute module, the first step is to set spare marker 107 to a logical "1", thus marking that module as the substitute module. As long as no fault in either of the other memory modules M2 and M3 is detected, no address is stored in the address register 400 and the output of the comparator 500 connected to the select-spare bus 200 is low (at logical "0"). As a result, and unless enabled via its other input, the output of the OR-gate 111 which enables the data store 21 remains low and hence the data store 21 inaccessible.

When a fault in one of the memory modules (say M3) is detected, the CPU enters the address of the memory module M3 into the address register 400 and simultaneously sets the spare-in-use bit in that register to "1" (or high). Thus the spare-in-use bus 300 now is at a logical high.

The inverter 105 in the address decoder logic unit 10 inverts the logical high of the spare-in-use bus 300 to a logical low, and hence, the output of the OR-gate 104, unless otherwise driven by the AND-gate 106, remains at a logical low. The AND-gate 103 is thus disabled even when the comparator 102 indicates a match in addresses. The data store 21 could not, therefore, be enabled when the address of the memory module 1 is called. Memory module M1 (marked as substitute or spare module) has thus been inhibited from responding to its address.

In its present system, the (substitute)

memory module M1 is loaded at this point with data identical to that in the faulty memory module M3. Such data is obtained from a standby magnetic tape unit MT in Figure 1 containing the vital system data. The arrangement is such that any data already stored in the memory module M1 is erased in the process of loading the module M1 with data from the tape unit MT. The tape unit itself could not be used instead of the faulty memory module M3 because data retrieval from tape is usually slow. Of course, other means may be used in this process of loading the memory module M1 with the necessary data. For example, the present system being a telephone system, it could request that the data be transmitted over the telephone lines from a remote storage location.

As various memory module addresses appear on the address bus 100 the comparator 500 continuously compares them with the contents of the address register 400. When the address of the nowfaulty memory module M3 appears on the bus 100 the comparator indicates a match on the select-spare bus 200, thereby enabling the AND-gate 110 (the other input of which is at "1" through the setting of spare marker 107), which in turn enables the OR-gate 111 and hence the data store 21. The memory module M1, marked as a spare, is thus selected to respond instead of the faulty memory module M3.

WHAT WE CLAIM IS:—

1. In a data processing system having a plurality of separately callable memory modules each having an address, a method of substituting one memory module for another, comprising the steps of:

(a) electronically marking one memory module as a substitute module;

(b) entering into a register the address of another memory module upon detection of a fault in that other memory module;

(c) inhibiting said one memory module from responding to its address;

(d) continuously comparing called memory module addresses with the address in said register; and

(e) upon occurrence of a match in the comparison of step (d), selecting said one memory module to respond instead of the called memory module.

2. The method of claim 1 further comprising the step of loading said one memory module from an auxiliary data source after fault detection in said another memory module with data substantially identical to that stored in said another memory module prior to said fault detection.

3. The method of claim 2 wherein any information in said one memory module is erased in the process of loading the same with said data.

4. In a data processing system performing supervision and control functions within a multi-line, multi-station telephone exchange system, a method of increasing the reliability of said telephone exchange system by permitting substitution of one memory module for another memory module said memory modules being two of a plurality of separately callable memory modules each having a unique address, said method comprising, in order, the steps of:

(a) electronically marking said one memory module as a substitute module;

(b) entering into a register the address of said another memory module upon detection of a fault therein by said data processing system;

(c) inhibiting said one memory module from responding to its unique address;

(d) continuously comparing called unique addresses of memory modules with the address stored in said register; and

(e) upon occurrence of a match between said stored addresses and one of said called unique addresses, selecting said one memory module to respond instead of said another memory module.

5. The method of claim 4 further comprising after step (c) the step of:

(f) loading said one memory module from a standby data store with data substantially identical to that stored in said another memory module prior to said fault detection.

6. The method of claim 5 wherein any data stored in said one memory module prior to said loading step is not preserved after said loading step.

7. A method substantially as described in conjunction with the drawings.

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Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1978.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1512220 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

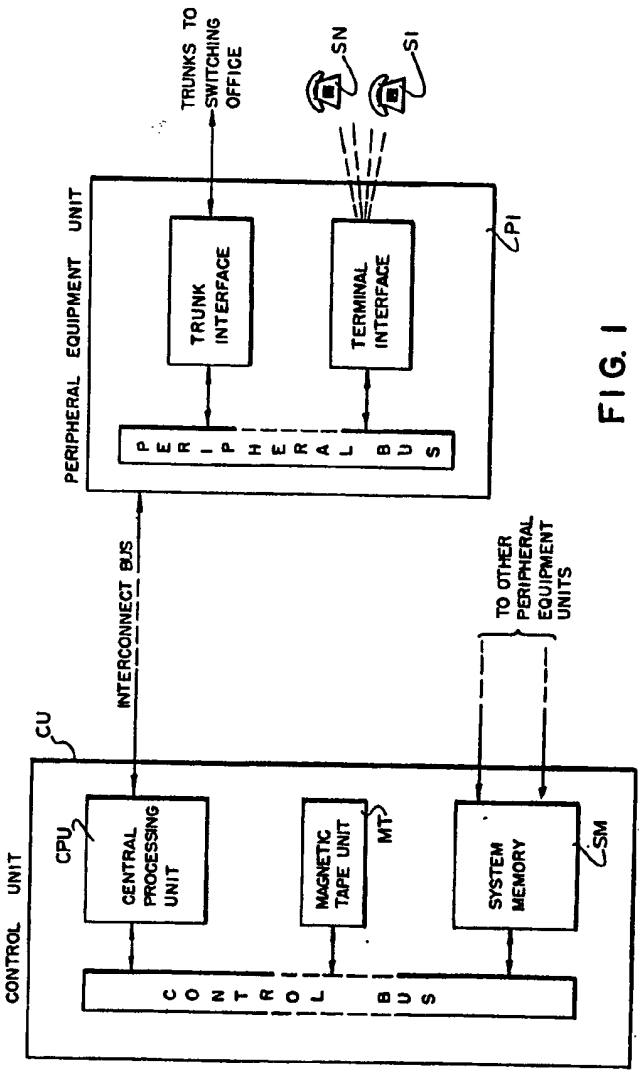

FIG. 1

1512220 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

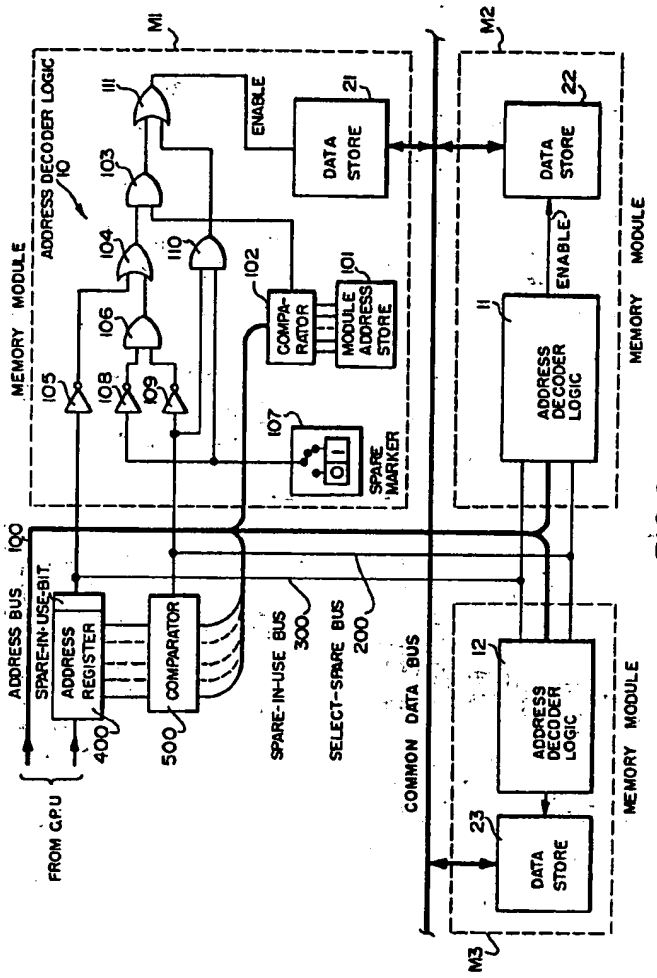

FIG. 2